REFERENCE MANUAL

Model 2108

TX01/RX01 Interconnect Modules

Manual Revision: 06/22/06
Manual Part Number: 2108RM002
Instrument Part Number: 30100/30200

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An EADS North America Defense Company

CERTIFICATION

Talon Instruments certifies that this product met its published specifications at the time of shipment from the factory.

WARRANTY

Talon Instruments products are warranted against defects in materials and workmanship as follows:

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(b) Ninety days for cables and adapters.

During the warranty period, Talon Instruments will, at its option, either repair or replace products which prove to be defective.

For warranty service or repair, this product must be returned to the Talon Instruments factory. Buyer shall prepay shipping charges to the factory and Talon Instruments shall pay shipping charges to return the product to the Buyer. However, Buyer shall pay all shipping charges, duties, and taxes for products returned to Talon Instruments from another country.

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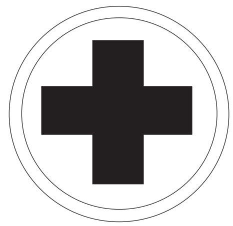
SAFETY FIRST



PROTECT YOURSELF AND THE EQUIPMENT.
Follow these precautions:

- Don’t bypass the chassis’ power cord’s ground lead with two-wire extension cords or plug adapters.
- Don't disconnect the green and yellow safety-earth-ground wire that connects the ground lug of the chassis power receptacle to the chassis ground terminal.
- Don't energize the chassis until directed to by the installation instructions.
- Don't repair the instrument unless you are a qualified electronics technician and have instructions from Talon Instruments.
- Pay attention to the **WARNING** statements. They point out situations that can cause injury or death.
- Pay attention to the **CAUTION** statements. They point out situations that can cause equipment damage.
- Use ESD static control procedures when handling the 2108 or any of its modules.

Table of Contents

List of Figures

List of Tables

1 TX01/RX01 Interconnect Modules

Just as each serial interface has unique data format and bit format characteristics, each interface also has unique electrical line driver/receiver characteristics. These characteristics vary from output voltage levels, output slew rates, bipolar or trinary signals, differential output signals and more. The TX01 and RX01 were developed to address all these characteristics for interfaces which require variable voltage input/output levels of up to +/- 15 volts.

1.1 2108 TX01 Module

The TX01 shown below provides 8 +/- 15V variable voltage outputs. The Transmitter Interconnect Modules provide the user with drivers to meet the electrical requirements of the UUT. Variable voltage drivers may be programmed to meet a wide range of signal levels from ECL to +/- 15V in 20mV increments. In addition, drivers may be programmed as bipolar, differential or trinary. Custom modules can be easily deleloped if off-the-shelf modules do not meet the user’s requirements.

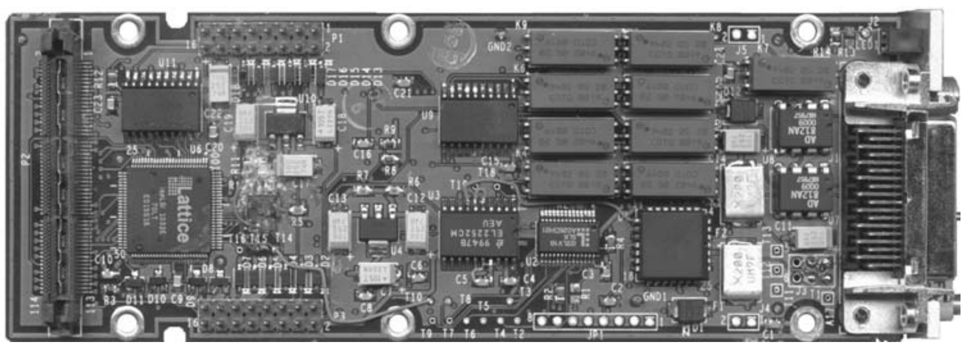


Figure 1-3 TX01 Bottom View

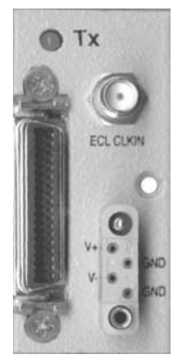


Figure 1-2 2108 TX01 Front View

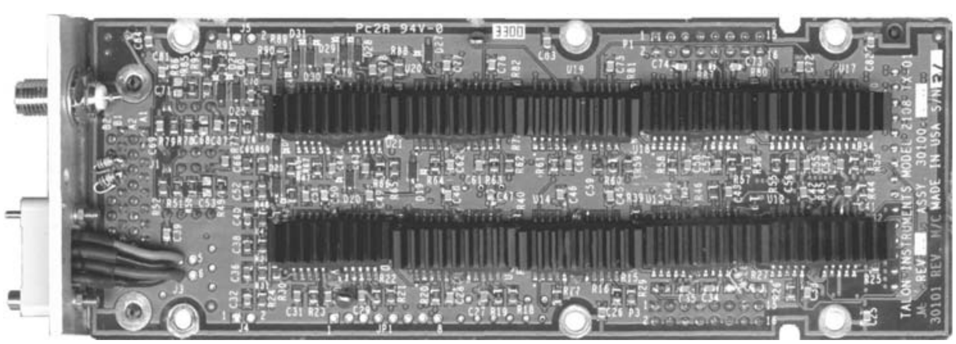


Figure 1-1 TX01 Top View

1.2 2108 RX01 Module

The RX01 shown below provides a single channel for recording serial data. The Receiver Interconnect Modules provide for the physical connection to the UUT. The voltage detection range may be set as high as –15V to +15V with standard modules. Signal types may be programmed as bipolar or differential.

Software selectable impedance is provided. Data rates to 100 Mbps are supported. Custom modules can be easily deleloped in those cases where standard modules do not meet the user's requirements.

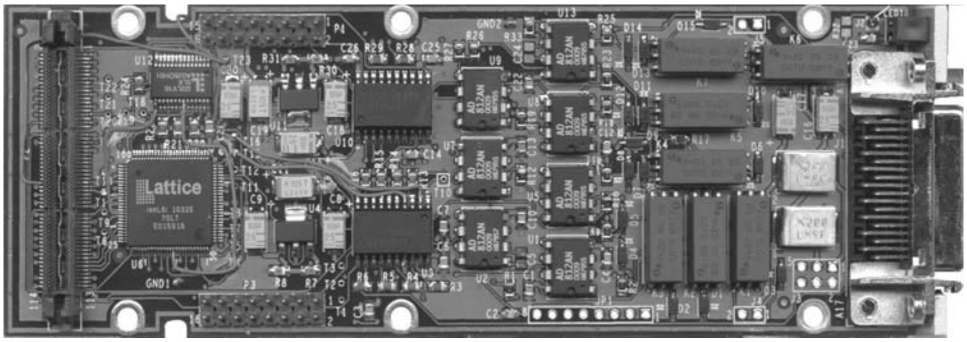


Figure 1-6 RX01 Bottom View

Figure 1-5 RX01 Front View

Figure 1-4 RX01 Top View

2 Specifications

The following sections list the specifications of the 2108 TX01/RX01 modules.

2.1 General

TX01

- TxSig Outputs
  - Configuration TxSig1/TxSig2 .... Bipolar/Differential/Trinary
  - Configuration TxSig3-TxSig8 .... Bipolar
  - VOH max. .... +15V
  - VOH min. .... VOL
  - VOL max. .... VOH
  - VOL min. .... -15V
  - Output Level Resolution 20mV
  - Output Level Accuracy 50mV
  - Source/Sink 50mA
  - Voltage Swing VOH to VOL 24V
  - Output Impedance TxSig1/TxSig2 .... 15/50Ω Selectable
  - Output Impedance TxSig3-TxSig8 .... 50Ω
  - Slew Rate .... 0.15V/ns to 1V/ns programmable
  - Bit Rate 100Mbps
- TxClkIn1
  - Configuration .... Bipolar ECL
  - Input Impedance .... 51Ω to -2V
  - Frequency max. 200MHz
- TxClkIn2
  - Configuration .... Single Threshold Bipolar/Differential
  - VIH max .... +15V
  - VIH min .... -15V
  - Threshold Resolution 20mV
  - Threshold Accuracy 50mV
  - Input Impedance .... 100K/100Ω Selectable
  - Frequency max. 50MHz

RX01

- RxData Inputs
  - Configuration .... Dual Threshold Bipolar/Differential
  - VIH max. .... +15V
  - VIH min. VIL
  - VIL max. .... VIH
  - VIL min. .... -15V
  - Threshold Resolution 20mV
  - Threshold Accuracy 50mV
  - Input Impedance .... 100K/100Ω Selectable
  - Data Rate. 100Mbps
  - Configuration
- RxClkIn1
  - Configuration .... Bipolar ECL
  - Input Impedance .... 51Ω to -2V
  - Frequency max. 200MHz
- RxQual/RxClkIn2 Inputs
  - Configuration .... Single Threshold Bipolar/Differential
  - VIH max. .... +15V
  - VIH min. .... -15V
  - Threshold Resolution 20mV
  - Threshold Accuracy 50mV
  - Input Impedance .... 100K/100Ω Selectable
  - RxQual Data Rate. 100Mbps
  - RxClkIn2 Data Rate. 50MHz
- Voltage Detection Range
  - Common Mode .... +/- 15V
  - Bipolar .... 0.8 to 30V
  - Differential .... 0.4 to 15V

2.2 Environmental

Temperature Range

Operating	0° C to +50° C
Storage	-40° C to +70° C (RH not controlled)

Altitude

Operating	Sea level to 10,000 ft.
Storage	Sea level to 40,000 ft.

Relative Humidity (non condensing)

0^oC to $+10^oC$	not controlled
$+11^oC$ to $+30^oC$	95+/-5%RH
$+31^oC$ to $+40^oC$	75+/-5%RH
$+41^oC$ to $+50^oC$	45+/-5%RH

2.3 Power Requirements

The following sections describe the VXI and front panel power requirements of the 2108 TX01 and RX01 interconnect modules.

2.3.1 VXI Power Requirements

The VXI backplane power requirements are listed in table 2-1 below.

Voltage	TX01	RX01
	Peak (Amps)	Peak (Amps)
+5V	0.550	0.425
-5.2V	0.150	0.150
-2V	0	0
+12V	0	0
-12V	0	0
+24V	0.055	0.200
-24V	0.055	0.200

Table 2-1 VXI Backplane Power Requirements

2.3.2 Front Panel Power Requirements

The following lists the TX01 front panel V+ and V- voltage requirements.

V+ maximum .... +20V
V+ minimum .... +7V
V- maximum .... -7V
V- minimum .... -20V
V+ to V- Voltage max. 32V
V+ headroom from VOH .... +4V
V- headroom from VOL .... -4V
V+ current max 1A
V- current max 1A
V+ current disabled 210mA
V- current disabled 235mA

2.4 Cooling Requirements

The total power dissipated by the Model 2108 is equal to the sum of the individual power dissipations of its modular components. The following sections give maximum and typical power dissipation numbers for the TX01 and RX01 modules. Refer to the Model 2108 Reference manual for the cooling requirement worksheet where these dissipation numbers will be used.

2.4.1 TX01 Power Dissipation

The TX01 power dissipation is the sum of the power off (P_{off}), power on (P_{on}) and the load power (P_{load}) and can be expressed by the following equations:

P_{off} = (+5V X 550mA) + (| -5.2V| X 150mA) + (+24V X 55mA) + (|-24V| X 55mA) + (V+ X 210mA) + (|V-| X 235mA)
P_{on} = (V+ X [(Number of Channels X 40ma) + 200mA]) + (|V-| X [(Number of Channels X 40ma) + 200mA])
P_{load} = [(V+ - VOH) + |(V- - VOL)|] / 2 X (Load Current) X (Number of Channels) X (Load Factor)

From these equations we can calculate maximum and typical power dissipation numbers.

For the maximum power dissipation we will use the following values:

V+ (+16V)
V- (-16V)

VOH (+1V)
VOL (-1V)
Number of Channels (8)
Load Current (50mA)
Load Factor (1)

$P_{total} = P_{off}$ (13.29W) $+P_{on}$ (16.64W) + P_{load} (6W)
35.93W

For the typical power dissipation we will use the following values:

V+ (+7V)
V- (-7V)
VOH (+2V)
VOL (-2V)
Number of Channels (2)
Load Current (25mA)
Load Factor (0.25)

$P_{total} = P_{off}$ (3.92W) $+P_{on}$ (9.29W) + P_{load} (63mW)
13.27W

2.4.2 RX01 Power Dissipation

The RX01 power dissipation can be expressed by the following equation:

P_{total} = (+5V X 425mA) + (|-5.2V| X 150mA) + (+24V X 200mA) + (|-24V| X 200mA)
12.5W

3 Jumpers/Testpoints

The following sections describe the jumpers for the 2108 TX01 and RX01 modules.

3.1 TX01 Jumpers/Testpoints

Figure 3-1 below shows the location of the jumpers and test points on the 2108 TX01 UUT interconnect module PCB, part number 30101 revision ‘N/C’.

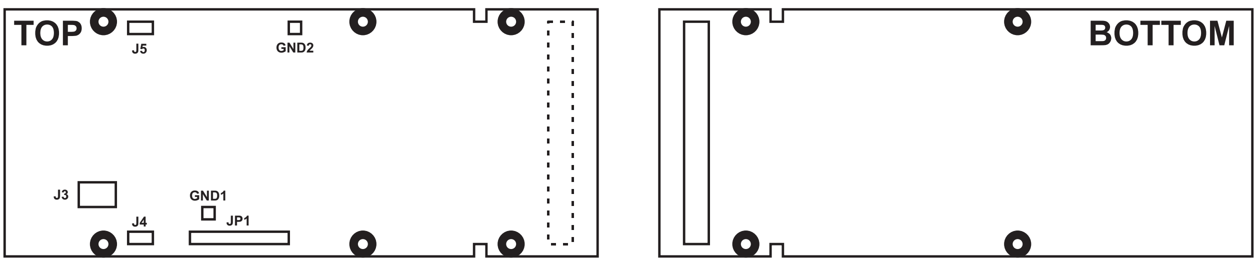


Figure 3-1 2108 TX01 Jumper/Testpoint Location

3.1.1 2108 TX01 Test Point Description

Table 3-1 describes the test points on the 2108 TX01.

Mnemonic	Description
GND1	Probe Signal Ground.
GND2	Probe Signal Ground.
JP1	In-circuit Program Port for U6.

Table 3-1 2108 TX01 Test Point Description

3.1.2 2108 TX01 Jumper Description

The following sections describe the 2108 TX01 jumpers.

3.1.2.1 Driver Voltage Source (J3)

This jumper is used to select the driver voltage source from either the front panel or the VXI backplane.

Factory default: Front panel selected.

Select the VXI backplane by installing a shunt between pins 3 and 5 (+12V) and pins 4 and 6 (-12V).

3.1.2.2 Channel Voltage Daisy Chain (J4, J5)

These jumpers chain the voltage buses (V+ and V-) to adjacent channels.

Factory default: Daisy chain not connected.

To connect the front panel power bus to adjacent channels install shunts between J5,J4 pin 1 and 2 to J4,J5 pin 1 and 2 of the adjacent UUT interface module.

3.2 RX01 Jumpers/Testpoints

Figure 3- below shows the location of the jumpers and test points on the 2108 RX01 UUT interface module PCB, part number 30201 revision 'A'.

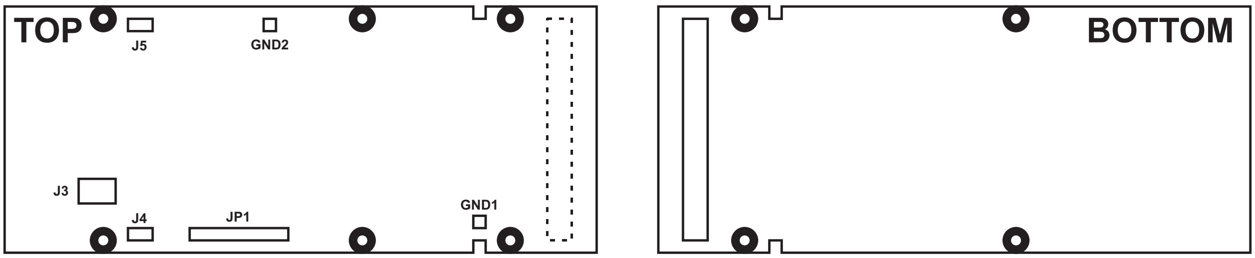


Figure 3-2 2108 RX01 Jumper/Testpoint Location

3.2.1 2108 RX01 Test Point Description

Table 3-2 describes the test points on the 2108 RX01.

Mnemonic	Description
GND1	Probe Signal Ground.
GND2	Probe Signal Ground.
JP1	In-circuit Program Port for U6.

Table 3-2 2108 RX01 Test Point Description

3.2.2 2108 RX01 Jumper Description

The following sections describe the 2108 RX01 jumpers.

3.2.2.1 Daisy Chain Voltage Source (J3)

This jumper is used to select the daisy chain voltage source as the VXI backplane.

Factory default: None selected.

Select the VXI backplane by installing a shunt between pins 3 and 5 (+12V) and pins 4 and 6 (-12V).

3.2.2.2 Channel Voltage Daisy Chain (J4, J5)

These jumpers chain the voltage buses (V+ and V-) to adjacent channels.

Factory default: Daisy chain not connected.

To connect the bus to adjacent channels install shunts between J5,J4 pin 1 and 2 to J4,J5 pin 1 and 2 of the adjacent UUT interface module.

V+ and V- are not used on the RX01 module. The daisy chain is provided to bridge V+ and V- across the interconnect modules.

4 Front Panel

The following describes the pinout and signal description of the Model 2108 TX01/RX01 UUT interconnect modules.

4.1 TX01 Front Panel

Figure 4-1 below illustrates the TX01 front panel.

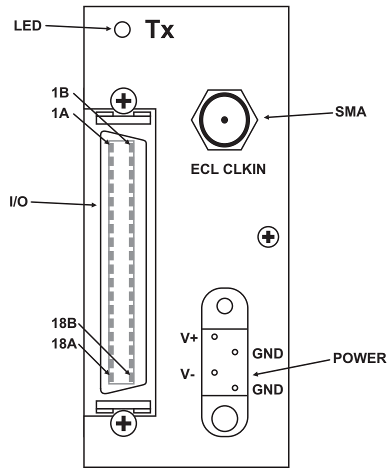


Figure 4-1 TX01 Front Panel

The TX01 front panel is comprised of four elements, LED, SMA, I/O, POWER.

The following sections describes each of these elements.

4.1.1 TX01 Front Panel LED

The front panel LED is a bi-colored indicator of the following conditions:

GREEN	The 2108TX is currently transmitting a CMT in the RUN state.
RED	The TX01 drivers have shut down due to drive fault condition on one or more of the programmable drivers or an over temperature.

4.1.2 TX01 Front Panel SMA

The front panel SMA is used to input the ECL clock input signal (TxClkIn1).

4.1.3 TX01 Front Panel I/O

The front panel I/O connector (AMP P/N “2-178238-5”) is used to connect the 2108 to the UUT/ITA fixture.

Talon sells a shielded twisted pair three foot cable assembly P/N “2108/300” that has a mating connector on one side and open ended on the other.

Table 4-2 below list the pinout of the TX01 I/O connector.

Pin Number	Signal	Default Source	Description
2A	TxSig1	TxData	Programmable output with dynamic reference error.
4A	TxSig2	TxClkOut	Programmable output with dynamic reference error.
6A	TxSig3	TxMarker1	Static enable programmable output.
8A	TxSig4	TxMarker2	Static enable programmable output.
10A	TxSig5	TxFlagOut1	Static enable programmable output.
12A	TxSig6	TxFlagOut2	Static enable programmable output.
14A	TxSig7	TxSyncPulse	Static enable programmable output.
16A	TxSig8	TxBusy	Static enable programmable output.
2B	TxFlagIn1		TTL Input flag one.
4B	TxFlagIn2		TTL Input flag two.
6B	TxClkIn2+		Programmable clock positive input.
8B	TxClkIn2-		Programmable clock negative input.
10B	TxBusy		TTL transmitter busy flag.
12B	TxSyncPulse		TTL Transmitter sync pulse flag.
All other pins signal ground.			

Table 4-2 TX01 I/O Connector Pinout

4.1.4 TX01 Front Panel POWER

The front panel power connector (Positronix Industries P/N “SGM4FSCT0000”) is used to provide the V+ and V- supply voltages to the TX01 programmable drivers.

Talon sells a six foot cable assembly P/N “2108/304” that has a mating connector on one side and open ended on the other.

Table 4-1 below lists the pinout of the TX01 Power connector.

Pin Number	Signal	Description
A	V+	Positve supply voltage.
B	GND	Signal ground
C	V-	Negative supply voltage
D	GND	Signal ground

Table 4-1 TX01 Power Connector Pinout

4.2 RX01 Front Panel

Figure 4-2 below illustrates the RX01 front panel.

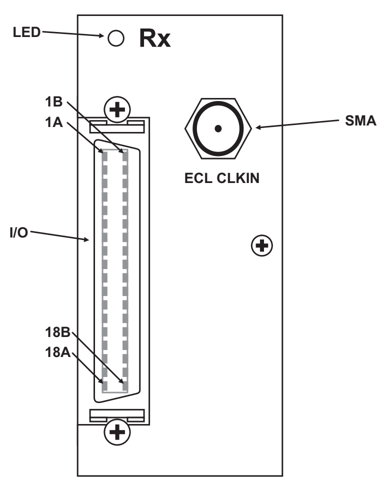


Figure 4-2 RX01 Front Panel

The RX01 front panel is comprised of three elements, LED, SMA, I/O.

The following sections describes each of these elements.

4.2.1 RX01 Front Panel LED

The front panel LED is a bi-colored indicator of the following conditions:

AMBER	The 2108RX is currently waiting for a trigger (armed).
GREEN	The 2108RX is currently recording post trigger data.

The front panel LED will only be active if RxBusy is selected as RxSig2 and RxArm as RxSig1.

4.2.2 RX01 Front Panel SMA

The front panel SMA is used to input the ECL clock input signal (RxClkIn1).

4.2.3 RX01 Front Panel I/O

The front panel I/O connector (AMP P/N “2-178238-5”) is used to connect the 2108 to the UUT/ITA fixture.

Talon sells a shielded twisted pair three foot cable assembly P/N “2108/300” that has a mating connector on one side and open ended on the other.

Table 4-3 below list the pinout of the RX01 I/O connector.

Pin Number	Signal	Default Source	Description
2A	RxData+		Positive data input.
4A	RxData-		Negative data input.
6A	RxClkIn2+		Positive clock input
8A	RxClkIn2-		Negative clock input
10A	RxQual1+		Positive qualifier one.
12A	RxQual1-		Negative qualifier one.
14A	RxQual2+		Positive qualifier two.
16A	RxQual2-		Negative qualifier two.
18A	RxSig1	RxArm	TTL receiver signal 1.
2B	RxTrigValid		TTL trigger valid flag.
4B	RxTrigNum0		TTL trigger number zero.
6B	RxTreigNum1		TTL trigger number two.
8B	RxTrigNum2		TTL trigger number three.
10B	RxTrigNum3		TTL trigger number four.
12B	RxG0Val		TTL receiver good zero data.
14B	RxG1Val		TTL receiver good one data.
16B	RxClkOut		TTL receiver clock.
18B	RxSig2	RxBusy	TTL receiver signal 2.
All other pins signal ground.			

Table 4-3 RX01 I/O Connector Pinout

5 Functional Description

The following sections describe the TX01/RX01 functionality.

5.1 TX01

The TX01 is a UUT interconnect module for the 2108TX transmitter module. It mounts on the 2108 Baseboard and provides the I/O translation between the UUT and the 2108TX module.

The TX01 provides variable +/- 15 volt I/O and can operate at data rates up to 100 Mbps.

5.1.1 TX01 Output Signals

There are eight voltage programmable outputs (TxSig1 through TxSig8) for the 2108TX01 and two TTL outputs (TxBusy and TxSyncPulse). All eight voltage programmable outputs can be bipolar, or paired together to make 4 differential outputs. They can all have a swing of up to 24 volts within the range of +/-15 volts with programmable slew rate. Each output can drive +/- 50 mA. The TxSig1 and TxSig2 outputs have dynamic enables and their outputs can be Tri-stated or Driven to a third state. Output error conditions can also be programmed.

The choices for each signal are the true or complemented state of the following:

TxData
TxMarker1
TxMarker2
TxFlagOut1
TxFlagOut2
TxClkOut
TxStrobe
TxBusy
TxSyncPulse

5.1.1.1 Bipolar Output Signals

Figure 5-1 depicts an output driver when configured for a bipolar output signal. The “inject error” capability only applies to the TxSig1 and TxSig2 outputs.

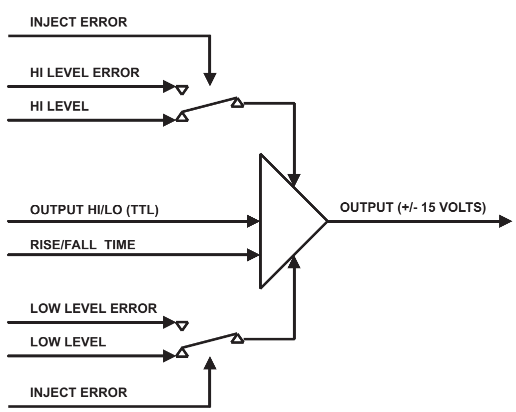


Figure 5-1 Bipolar Driver Configuration

Figure 5-4 depicts a typical output waveform for the bipolar output configuration.

Figure 5-4 Bipolar Configuration Waveform

5.1.1.2 Trinary Output Signals

Trinary drivers may be programmed in one of two modes: a Passive (Tri-State) 3rd state or a Driven (low impedance) 3rd state.

5.1.1.2.1 Passive Tri State Drivers

The Passive Tri-state driver configuration operates identically to the bipolar configuration, with an additional control signal which allows the driver to drive to the tri-state condition. The output impedance in the Tri-state mode is 100k ohms. Figure 5-2 depicts the block diagram for this configuration.

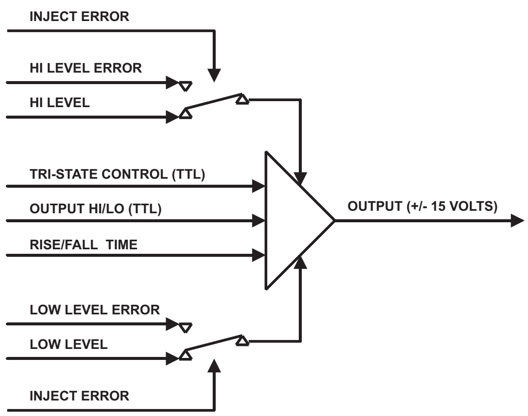


Figure 5-2 Bipolar Tri-State Configuration

Figure 5-3 depicts a typical waveform for the tri-state driver.

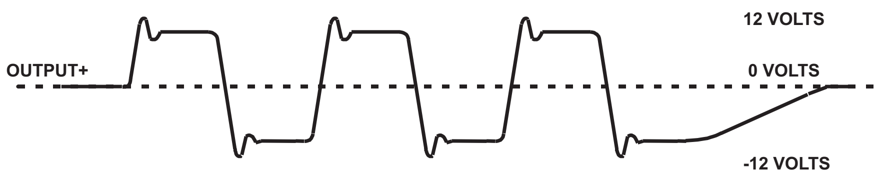


Figure 5-3 Bipolar Tri-State Configuration Waveform

Only TxSig1 and TxSig2 have passive tri-state control.

Note: The tristate level of the signal is determined by the user's termination voltage. Figure 5-3 depicts a waveform connected to ground through a large value resistor. Without user termination, a tri-state output may wander anywhere between V+ & V-.

5.1.1.2.2 Driven 3rd State Driver

The Driven 3rd state driver configuration employs a second driver. The second driver, which generates the third state, is selected by a control signal. The third state may be any voltage between +/- 15 volts. This capability, including error injection, applies to the TxSig1 output only. Figure 5-6 depicts the block diagram for the active 3rd state driver.

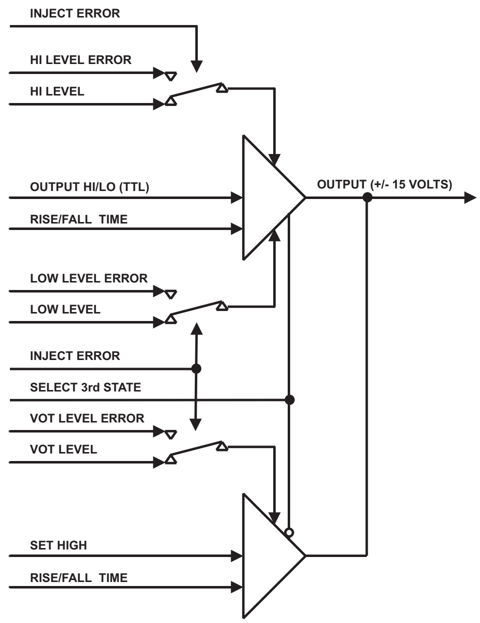


Figure 5-6 Bipolar with Active 3rd State

Figure 5-5 depicts a typical waveform for the active 3 rd state driver (3 rd state is set to 0 volts).

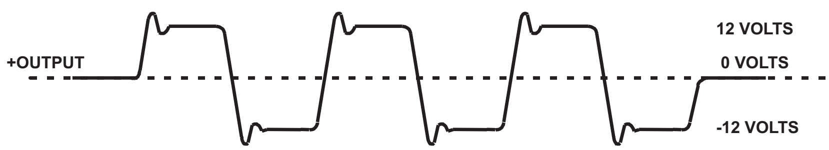


Figure 5-5 Bipolar with Driven 3rd State Waveform

5.1.1.3 Differential Drivers

The 2108TX01 may also be programmed to emulate differential drivers. Two identical bipolar driver circuits are used to provide both halves of the differential pair, therefore, the driver characteristics for each signal is the same as a single bipolar driver.

Figure 5-8 depicts the block diagram for the differential driver. The “INJECT ERROR” capability applies to the TxSig1 and TxSig2 outputs only.

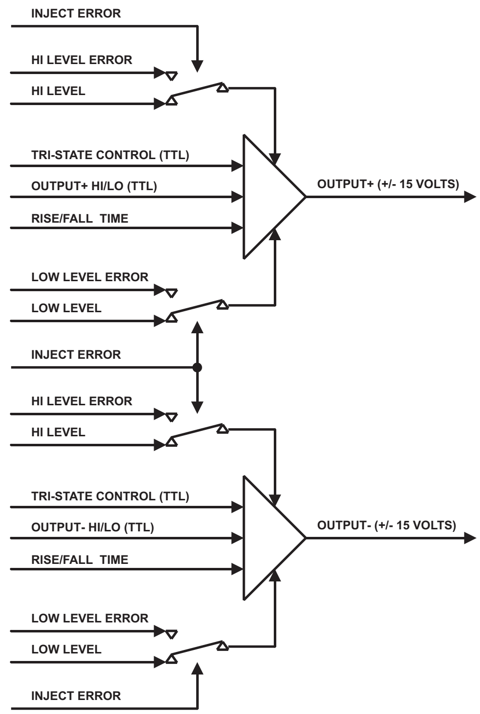


Figure 5-8 Differential Mode

Figure 5-7 depicts a typical waveform for the differential output configuration.

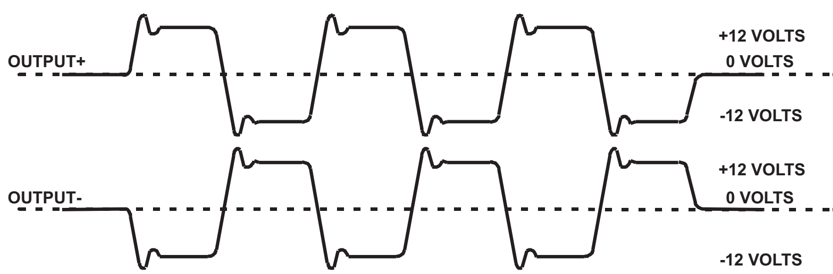


Figure 5-7 Differential Mode Waveform

The error voltage on either one or both drivers may be programmed on a bit, several bits, or on scattered groups of bits. The “TRI-STATE CONTROL” allows for a Tri-state condition on the output.

5.1.1.4 Output Voltage Errors (TxSig1 and TxSig2 only)

In the bipolar mode, error voltages may be selected for the high-level output voltage, the low level output voltage and/or the driven third state output voltage (if enabled). Error conditions may be programmed on a bit, several bits or on scattered groups of bits. Figure 5-11 depicts a typical error waveform.

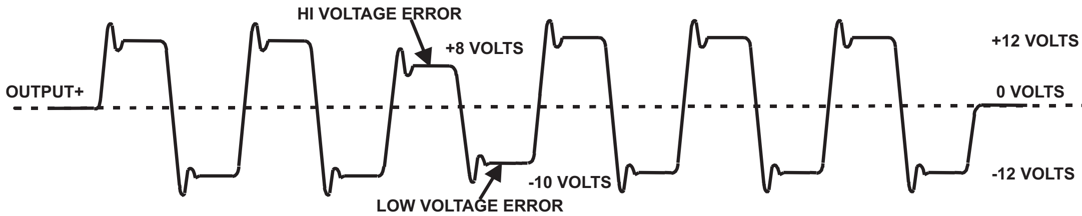


Figure 5-11 Bipolar Waveform with Error

In the Differential Mode, high and low level output voltage errors may also be programmed.

5.1.1.5 Output Impedance

The output impedance of TxSig1 and TxSig2 drivers is typically 15 ohms. The user may also select an additional 35 ohm series resistor, yielding approximately a 50 ohm series output impedance, Figure 5-9. TxSig3 through TxSig8 have a fixed 50 ohm series output impedance.

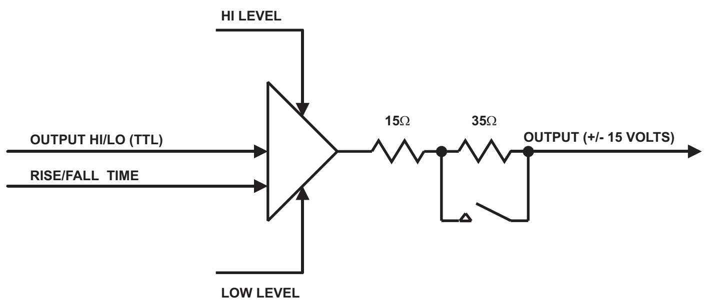


Figure 5-9 TxSig1/TxSig2 Output Impedance

Note 1: If the 50 ohm output impedance is selected and the output is also terminated with 50 ohms to ground, it would require a 10 volt output at the driver to generate a 5 volt signal at the termination.

Note 2: When the output is terminated with 50 ohms, the maximum output voltage will be limited because of the maximum drive current capability (10V in this example).

5.1.1.6 Output Slew Rate

The output slew rate of these drivers can be programmed to cover the range of ~1 V/ns to ~0.15 V/ns unloaded. See figure 5-10. The slew rate for the “error condition” can be set independently.

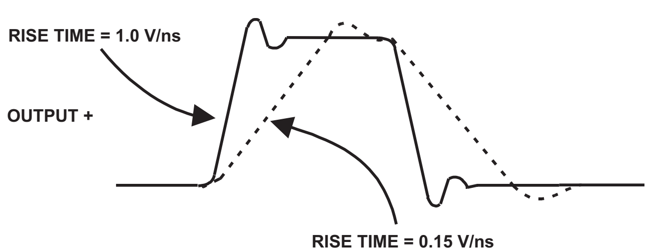


Figure 5-10 Driver Slew Rate

5.1.1.7 Output Bit Rate (and Clock Output Rate)

The maximum practical BIT rate for any of the programmable outputs is a function of the programmed output voltage swing. Since the Clock Output has two edge transitions for each Data bit, the maximum Clock rate is less for the same swing.

Table 5-1 defines the maximum Bit and Clock rates for three different voltage output levels (fastest slew rate).

Voltage Swing	Maximum Data Rate (Mbps)	Maximum Clock Rate (MHz)
5V	100	50
10V	80	40
20V	50	25

Table 5-1 Output Bit Rate vs. Output Voltage Swing

5.1.1.8 Over-Current Protection on the Variable Voltage Output Drivers

Exceeding the drive current on any one of the output drivers causes a “driver fault” which powers down all the output drivers and turns the front panel indicator Red. This latched condition is reset by reading the Interrupt Event Register, see Appendix B section 1.2.3.

5.1.1.9 TTL Outputs

There are two TTL driven outputs, TxBusy and TxSyncPulse driven by a 74AS244.

5.1.1.10 Air Flow/Temperature Monitoring

The 2108TX01 utilizes high-powered output drivers, which dissipate considerable heat when powered-up and active. Adequate airflow must therefore be provided. A temperature sensor is provided which monitors a combination of the air and board temperature. A temperature greater than 80°C will power-down the drivers, generate a drive fault signal and turn the front panel indicator Red. This latched condition is reset by reading the Interrupt Event Register, see Appendix B section 1.2.3.

5.1.1.11 Bi-Directional Capabilities

The TxSig1 and TxSig2 Outputs (bipolar or differential) can be programmatically routed over to the adjacent 2108RX01 Data Inputs. This permits bi-directional communication with the users UUT over one data line. Typically, for this mode of operation, the Data Line would be terminated at the 2108RX01 and the users UUT. The selected clock input (TxClkIn1 or TxClkIn2) can also be programmatically routed over to the adjacent 2108RX01.

5.1.2 2108TX01 Inputs

There is a variable threshold clock input (TxClkIn2), and ECL clock input (TxClkIn1) and two TTL Flag Inputs (TxFlagIn1 and TxFlagIn2). The TxClkIn2 input can be a bipolar or differential input and handle +/- 15 volt inputs or a 15 volt differential input (within a +/- 15 volt common mode range) up to 50 MHz. The TxClkIn1 ECL input can accommodate clock input frequencies up to 200 MHz.

5.1.2.1 TxClkIn2 Input (Variable Threshold)

The TxClkIn2 input may be a Bipolar or Differential input. A bipolar swing of from 0.8V to 30V or a differential input swing of 0.4 to 15V may be applied within the common mode range of +/- 15V. The input threshold level is programmable.

Each input has a 100KΩ pull down to ground, which is used to establish an input level (ground) for the inputs when a signal is not applied. This input also has an input termination resistor of 100Ω, which can be programmatically switched in between the inputs (in bipolar, it’s effectively from the TxClkIn2+ to ground).

> **CAUTION**
> **Since the INPUT- is grounded in the bipolar mode, the user is cautioned not to have a signal driving this input.**

The components for this “variable threshold” clock input are powered by the VXI chassis and do not use V+ or V-. Figure 5-12 shows the block diagram of the TxClkIn2 input circuit.

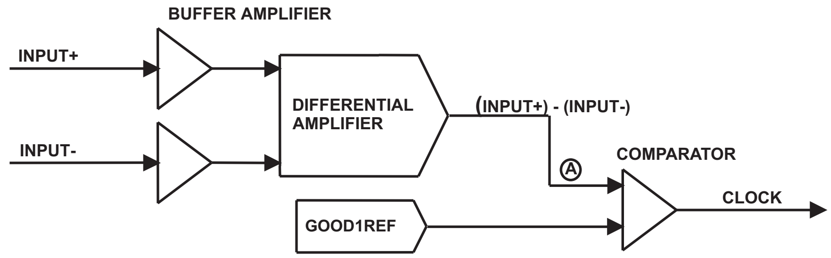


Figure 5-12 TxClkIn2 Input Diagram

The maximum operating rate can be attained by having limited input swings and by setting the threshold at mid swing. Table 5-2 lists some examples:

Input Type	Input Levels	Signal @ “A”	GOOD1REF	Max Frequency
Differential	5V	-5V to +5V	0V	50MHz
	15V	-15V to +15V	0V	25MHz
Bipolar	0V to +5V	0 to +5V	2.5V	50MHz
	-5V to 15V	-5V to +15V	5V	25MHz

Table 5-2 TxClkIn2 Input Examples

The inputs have limited protection from over-drive. This is especially needed for the case when the VXI chassis power is down, yet signals are being applied to the inputs by the user’s UUT. A 5V signal on the inputs when power is off on the VXI chassis will not cause damage.

5.1.2.2 TxClkIn1 Input (ECL)

The TxClkIn1 Input is provided for use when a clock input of greater than 50 MHz is required. This clock input will also have less jitter than the variable threshold clock input. It’s an ECL 10K compatible input with a fixed 50Ω termination to –2V. Optionally, the TxClkIn1 input may be terminated to –5.2V or not terminated at all (special order).

5.1.2.3 TTL Inputs

The Flag Inputs are standard TTL compatible inputs.

5.2 RX01

The RX01 is a UUT interconnect module for the 2108RX receiver module. It mounts on the 2108 Baseboard and provides the I/O translation between the UUT and the 2108RX.

5.2.1 RX01 Input Signals

There are four variable threshold inputs for the 2108RX01: RxData, RxClkIn2, RxQual1 and RxQual2 and one ECL input (RxClkIn1). All four variable inputs can be either Bipolar or Differential. A bipolar swing of from 0.8 to 30 V or a differential input swing of 0.4 to 15 V may be applied within the common mode range of +/- 15 V up to 100 Mbps (50 MHz for RxCLKIN1). The RxData input has a window comparator allowing both a GOOD “1” and a GOOD “0” threshold to be programmed. The other inputs have only a single programmable threshold. Each one can be programmed separately. The Bipolar mode of the receiver is a subset of the differential mode (the INPUT- is programmatically grounded).

5.2.1.1 Differential Input Signals

Figure 5-14 depicts the block diagram for the RxData inputs.

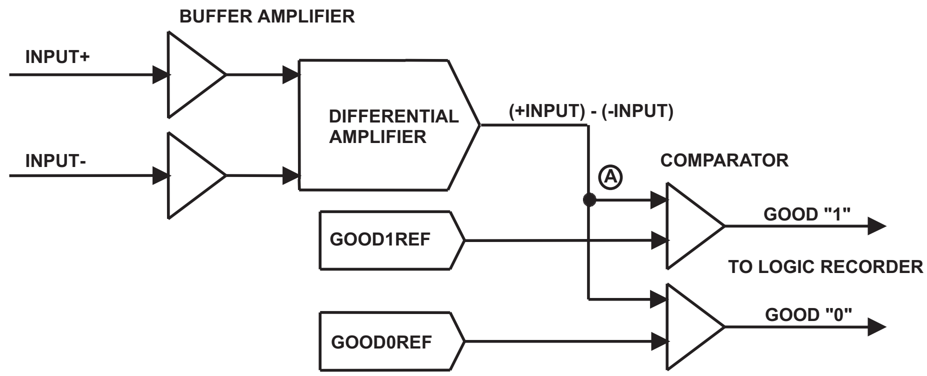


Figure 5-14 Differential RxData Configuration

The GOOD “1” comparator generates a logic “1” (true) signal if the differential signal is greater than a preprogrammed threshold reference signal, GOOD1REF. Similarly, the GOOD “0” comparator generates a logic “1” (true) signal if the differential signal is less than the preprogrammed threshold reference signal, GOOD0REF.

For example, assume the input differential signals +INPUT and -INPUT are + 5 volts and –5 volts respectively. The signal waveforms would look as depicted in Figure 5-13.

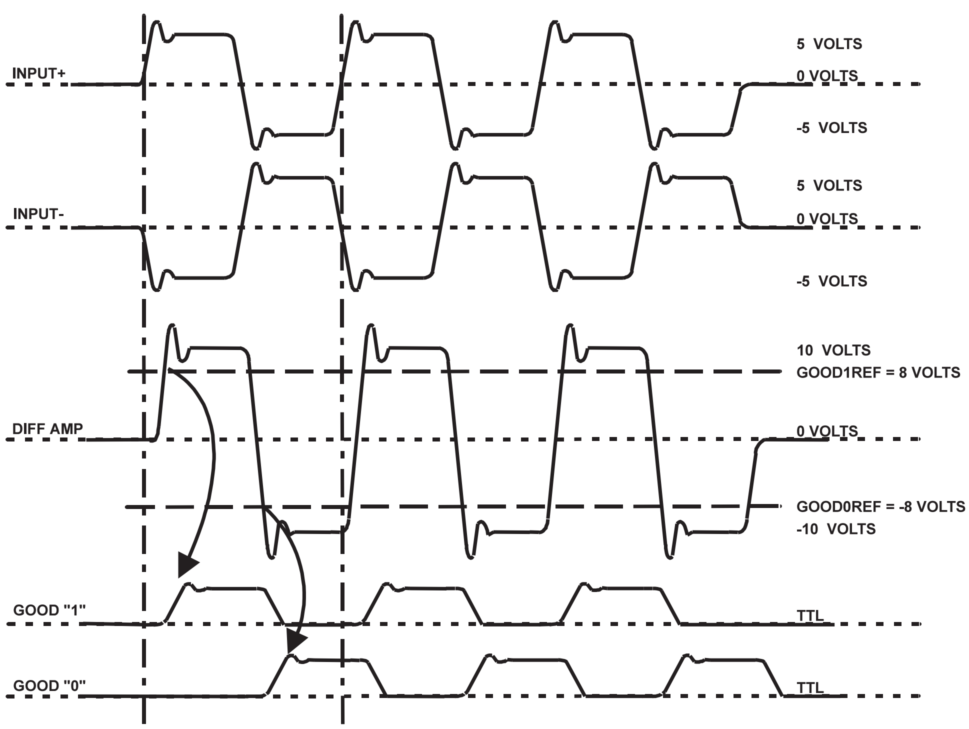


Figure 5-13 Differential Input Waveform

Assuming the GOOD1REF is set to 8 volts and the GOOD0REF is set to –8 volts, a GOOD “1” signal will be true when the difference between the INPUT+ signal and the INPUT- signal is greater than positive 8 volts. The GOOD “0” signal will be true when the difference between the INPUT+ signal and INPUT- signal is less than negative 8 volts.

The RxClkIn2, RxQual1 and RxQual2 input configurations are identical except they use a single GOOD1REF threshold signal.

5.2.1.2 Bipolar Input Signals

For bipolar input signals, the INPUT- signal is programmatically connected to ground. Therefore, the output of the differential amplifier will equal the INPUT+ signal. Figure 5-16 depicts the signals for the Input, the differential amplifier and the comparator signals for a bipolar +/-5 volt input signal.

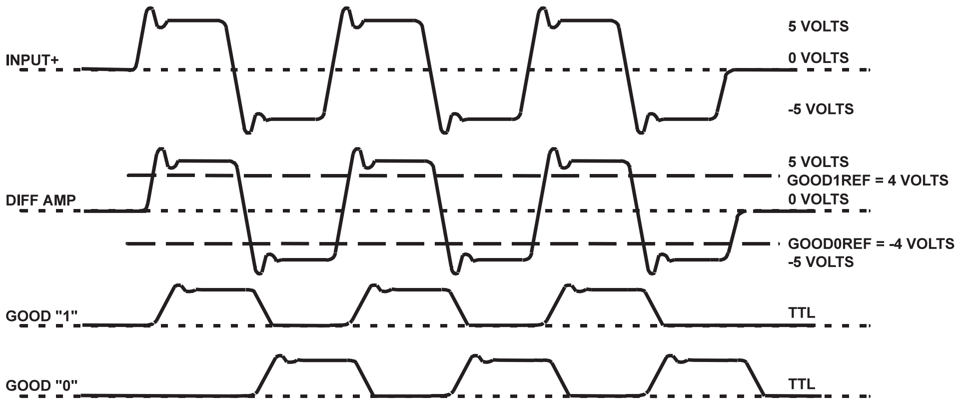


Figure 5-16 Bipolar Input Waveform

Figure 5-15 depicts the respective waveforms for a signal with TTL levels.

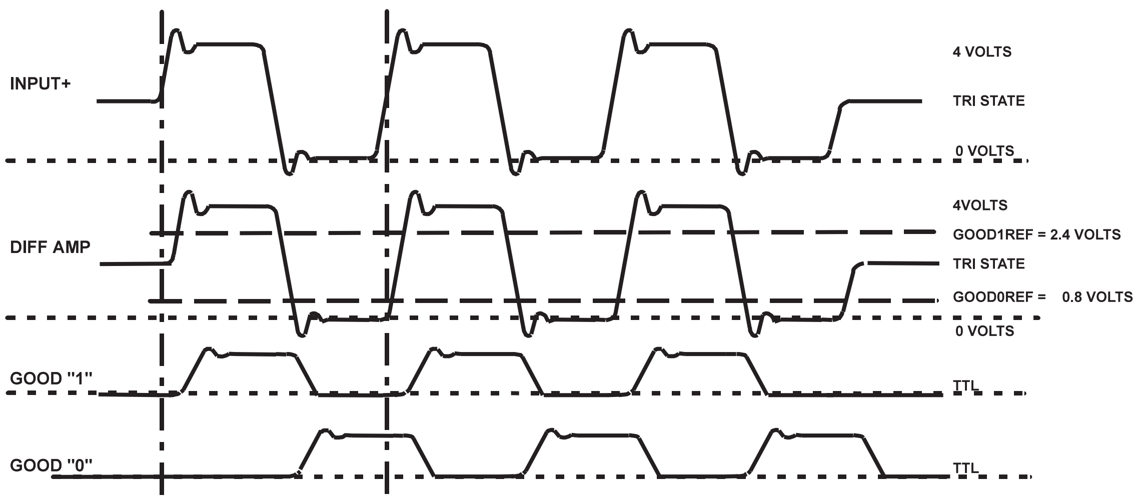


Figure 5-15 Bipolar Input TTL Levels

5.2.1.3 RxClkIn1 Input (ECL)

The RxClkIn1 input is provided for use when a clock input of greater than 50 MHz is required. This clock input will also have less jitter than the “programmable” clock input. It’s an ECL 10K compatible input with a fixed 50Ω termination to -2V. Optionally, the RxClkIn1 input may be terminated to -5.2V or not terminated at all (special order).

5.2.1.4 Input Impedance

Each input has a 100KΩ resistor to ground, which is used to establish an input level (ground) for the inputs when a signal is not applied. A 100Ω termination may also be programmatically switched in between the inputs (in bipolar, it’s effectively from the INPUT+ to ground).

CAUTION
Since the INPUT- is grounded in the bipolar mode, the user is cautioned not to have a signal driving this input.

5.2.1.5 Performance

The amplifiers and comparators used on this module have a slew rate capability of greater than 1V/ns. The input signal must have comparable slew rate in order to realize maximum performance. Using the 2108TX01 as a data source, the following Data rates can be accommodated:

Input Type	Input Levels	Signal @ "A"	Thresholds	Max Input Freq
Differential	5V	-5 to +5	0V	100Mbps
	5V	-5 to +5	-4V, +4V	50Mbps
	15V	-15 to +15	0V	50Mbps
	15V	-15 to +15	-9V, +9V	25Mbps
Bipolar	0V to 5V	0V to 5V	+2.5V	100Mbps
	0V to 5V	0V to 5V	+1V,+ 4V	50Mbps
	-5V to +15V	-5V to +15V	5V	50Mbps
	-5V to +15V	-5V to +15V	-1V, 11V	25Mbps

The RxClkIn2, because it has two transitions for each data bit, is necessarily restricted in performance. However, by limiting the input swing and setting the threshold at mid swing, performance can be maximized. Here are some examples:

Input Type	Input Levels	Signal @ "A"	VIH	Max Frequency
Differential	5V	-5V to +5V	0V	50MHz
	15V	-15V to +15V	0V	25MHz
Bipolar	0V to +5V	0 to +5V	2.5V	50MHz
	-5V to 15V	-5V to +15V	5V	25MHz

The Qualifier inputs (RxQual1 and RxQual2) have a performance as least as good as DATA, better if the threshold is set more mid swing.

5.2.1.6 Input Protection

The inputs have limited protection from over-drive. This is especially needed for the case when the VXI chassis power is down, yet signals are being applied to the inputs by the user's UUT. A 5V signal on the inputs when power is off on the VXI chassis will not cause damage.

5.2.1.7 Bi-directional Capabilities

A bi-directional mode of operation can be configured with the adjacent 2108TX01. When the 2108TX01 is in bi-directional mode, i.e. it has been programmed to enable the intermodule data and clock, the 2108RX01 can be programmed to select these inputs instead of its own front panel data and clock signals.

5.2.2 TTL Outputs

There are ten TTL outputs from the 2108RX01:

RxClkOut	RxTrigValid
RxG1Val	RxTrigNum0
RxG0Val	RxTrigNum1
RxSig1	RxTrigNum2
RxSig2	RxTrigNum3

The first three are driven by very fast, low skew, LVTTL drivers. The others are driven by a 74AS244. There's a programmable enable for these two groups of outputs so they may be turned off if not in use. The RxClkOut, RxG1Val and RxG0Val are especially useful, in that they are outputs from the 2108RX showing the digital signals which were derived from the input RxData and RxClkIn (via the amplifiers and comparators). Adjustable delay elements in the 2108Rx allow RxData and RxClkIn to be precisely aligned.

The trigger outputs (RxTrigValid, RxTrigNnum0, RxTrigNum1, RxTrigNum2, RxTrigNum3) indicate when a trigger occurs and the trigger number. RxSig1 and RxSig2 outputs are user selectable in the 2108Rx and described below:

RxSig1:

RxArm (default)	Record sequence running and waiting for trigger.
RxBusy	Record sequence running.
RxWait	Waiting for TxACK from transmitter.
TxAck	Acknowledge signal from transmitter.
LostClk	Clocks error signal.
HFCR-ERR	High frequency clock recovery error.
MemABsy	Record memory bank A busy.
LFCR-DEV	Low frequency clock recovery deviation (too slow or fast).

RxSig2:

RxArm	Record sequence running and waiting for trigger
RxBusy (default)	Record sequence running.
TrigDis	Trigger disabled (post trigger or waiting for TxACK).
TxAck	Acknowledge signal from transmitter.
LostClk	Clocks error signal.
HFCR-ND	High frequency clock recovery error. Not enough data.
MemBBsy	Record memory bank B busy.
LFCR-ERR	Low frequency clock recovery deviation error.

5.2.3 LED Indicator

When RxSig1 is chosen to be “RxArm” and the RxSig2 is chosen to be “RxBusy”, the LED will be Green when “BUSY” and Amber if “ARMED” and “BUSY”.

5.2.4 Self-Clocking Data

The 2108RX has built in capabilities to recover a clock from the input DATA. Consult the 2108RX description for further details.

Appendix A Glossary

Bipolar	One signal represents a state.
Comparator	Compares an input signal with a reference level.
Differential	A pair of signals represent a state. Also, when one is at a high level the other is at a low level and vice-versa.
Driver fault	The output driver (for S1 thru S8) is shut down due to current overloading or over temperature.
ECL	Emitter Coupled Logic.
FlagIn	An input signal which the transmitter can query.
FlagOut	An output signal (level or pulse) which the transmitter can generate.
Good “0”	A signal generated when an input signal is less than VIL.
Good “1”	A signal generated when an input signal is greater than VIH.
HRCR	High Frequency Clock Recovery.
LED	Light Emitting Diode.
LFCR	Low Frequency Clock Recovery.
Marker	An output signal used to mark one or more portions of the output data stream.
Reference	A programmable DC voltage.
RX01	Model 1 Receiver Interconnect Module.
RxArm	Record sequence “ARMed” and waiting for a trigger.
RxBusy	Record sequence running.
RxCLKOUT	An output signal derived from “Clock In” (used to align data wrt clock).
RxG0Val	An output signal derived from “Good-0” (used to align data wrt clock).
RxG1Val	An output signal derived from “Good-1” (used to align data wrt clock).
RxTrigNumber	The particular trigger number which occurred for a particular trigger event.
RxTrigValid	Trigger valid signal generated by the receiver when a trigger has occurred.
RxWait	Receiver is waiting for an acknowledge of a Trig Valid.
Slew rate	Rate of change of an output transition (typ in V/ns).
SMA	A small screw-on RF connector.
SyncPulse	An output pulse which can be positioned in relation to the output data stream (typically used to synchronize another instrument).
TrigDis	Trigger disabled in the receiver (in post trigger or waiting for a TxAck).
Trinary	Three distinct output levels from a TX output.
Tri-state	From the drivers view this is a passive-non driven state that is high impedance. From the receivers view this is a state between VIL and VIH.
TX01	Model 1 Transmitter Interconnect Module.
TxAck	A signal from the transmitter sent to the receiver acknowledging that a trigger has been captured.
TxBusy	Transmitter running.
TxCLKOUT	Selected clock being output by the transmitter (can be inverted and delayed).
UUT	Unit Under Test.
V+	Positive supply voltage provided by the user.

V-	Negative supply voltage provided by the user.
VOH	A reference defining an Output High Level.
VOL	A reference defining an Output Low Level.
VOZ	A reference defining an Output third state level.
VIH	A reference defining an Input High Level.
VIL	A reference defining an Input Low Level.
VXI	VME Extensions for Instrumentation.

Appendix B Register Description

The following sections describes the register maps of the TX01 and RX01 interface modules.
Both the TX01 and the RX01 register segments are located in the “IFCREG” major segment, 100000h.

1 TX01 Register Map

The TX01 register segments are described below:

Register Segment Code (RSC)				Register Segment Name	Base Address IFCREG + RSC	Description
A18	A17	A16	A15			
0	0	0	1	CSREG	108000h	Control/Status Register
1	1	1	0	INTR	170000h	Interrupt Registers
1	1	1	1	MID	178000h	Module id

Table B-2 TX01 Register Segment List

1.1 TX01 Control/Status Register (CSREG, RW:108000$_h$)

Table B-1 lists the bit description of the Tx01 Control/Status register.

Bit #																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU								C1M	C1T	CG	TSE	S2B	S2T	S1B	S1T	NU			DF	IMCE	CS2	CS1	CS0	S8EN	S7EN	S6EN	S5EN	S4EN	S3EN	S2EN	S1EN

Table B-1 TX01 Control/Status Bit Description

Field Bit Definition:

S1EN-S8EN — Driver enable (1 = enabled, 0 = disabled).

CS0-CS2 — Clock Select Code

Bit 10	Bit 9	Bit 8	Clock
0	0	0	Disabled
0	1	0	TxClkIn1
0	1	1	TxClkIn2
1	1	0	/TxClkIn1
1	1	1	/TxClkIn2

IMCE — Inter module clock enable. (1 = enabled, 0 = disabled).
DF — Drive Fault (1 = drive fault true, 0 = false).
S1T — Signal One Termination (0 = 15Ω, 1 = 50Ω).
S1B — Signal One Bidirectional enable (1 = enabled, 0 = disabled).
S2T — Signal Two Termination (0 = 15Ω, 1 = 50Ω).
S2B — Signal Two Bidirectional enable (1 = enabled, 0 = disabled).
TSE — Third State Drive enable. (1 = enabled, 0 = disabled).
CG — Chassis ground (1 = relay connect signal and chassis ground, 0 = disconnect).
C1T — TxClkIn1 Termination (1 = enabled, 0 = disabled).
C1M — TxClkIn1 Mode (1 = Bipolar, 0 = Differential)

Notes:

1. DF occurs when the analog driver tries to source more than 60mA of current for longer than 1 uS or the air temperature exceeds 80°C. The DF flag is reset by reading the Interrupt Event Register (Appendix B section 1.2.3).

1.2 Bit Slice Interrupt Control Registers (INTR)

The interrupt control registers allow the user to map and enable interrupt generation.
The control registers are mapped as described below.

Address LSB					Name	Offset	Description
A4	A3	A2	A1	A0			
0	1	0	X	X	IRQEN	170008h	Interrupt Enable
0	1	1	X	X	INT	17000Ch	Interrupt Register
1	0	0	X	X	EVENT	170010h	Event Register

Table B-3 Interrupt Control Registers

1.2.1 Interrupt Event Enable Register (IRQEN:170008$_h$)

This register allows the user to program specific event to cause an interrupt.
Table B-4 lists the bit description of the event enable register.

Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU														TF	DF

Table B-4 Interrupt Event Enable Bit Definitions

Field/Bit Definition:

DF Drive Fault.
TF Temperature Fault.

Notes:

1. 0 = disable event interrupt, 1 = enable event interrupt

1.2.2 Interrupt Register (INT:17000C$_h$)

This register allows the user to query the current status of the interrupt bits.
Table B-5 lists the bit description of the interrupt register.

Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU														TF	DF

Table B-5 Interrupt Register Bit Definition

Field/Bit Definition:

DF Drive Fault flag (1 = drive fault true, 0 = false).
TF Temperature Fault flag (1 = temperature fault true, 0 = false).

Notes:

None

1.2.3 Interrupt Event Register (EVENT:170010$_h$)

This register allows the user to query the interrupt event status. This register is cleared after it is queried and the event is reset.

Table B-8 lists the bit description of the interrupt event register.

Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU														TF	DF

Table B-8 Event Register Bit Definition

Field/Bit Definition:

- DF — Drive Fault positive transition.
- TF — Temperature Fault positive transition.

Notes:

1. 1 = event true, 0 = event false.

1.3 TX01 Module Identification (MID, R:178000$_h$)

The revision register contains the transmitter front end revision/status code.
Table B-7 lists the bit description of the module identification register:

Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU								T/R	T/P	ID					

Table B-7 TX01 Module Identification Bit Description

Field Bit Definition:

- ID — Identification Code
- T/P — Test/Production flag (1 = Test, 0 = Production).
- T/R — Transmit/Receive (1 = Receiver, 0 = Transmitter).

Notes:

1. A read of the MID register for the TX01 will return a ‘1’.

2 RX01 Register Map

The RX01 register segments are described below:

Register Segment Code (RSC)				Register Segment Name	Base Address IFCREG + RSC	Description
A18	A17	A16	A15			
0	0	0	1	CSREG	108000h	Control/Status Register
1	1	1	1	MID	178000h	Module ID

Table B-6 RX01 Register Segment List

2.1 RX01 Control Register (CSREG, RW:108000$_h$)

This register is used to program/query the Rx01 Control register.

Table B-10 lists the bit description of the Rx01 control register.

Bit #																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU											LEDEN	CS1	CS0	TEN1	TEN0	NU			CG	FPEN-	IMEN-	FPEN+	IMEN+	Q2M	Q2T	Q1M	Q1T	CM	CT	DM	DT

Table B-10 RX01 Control Register Bit Description

Field Bit Definition:

DT RxData Termination (1 = enabled, 0 = disabled).
DM RxData Mode (1 = Bipolar, 0 = differential).
CT RxClkIn1 Termination (1 = enabled, 0 = disabled).
CM RxClkIn1 Mode (1 = Bipolar, 0 = differential).
Q1T RxQual1 Termination (1 = enabled, 0 = disabled).
Q1M RxQual1 Mode (1 = Bipolar, 0 = differential).
Q2T RxQual2 Termination (1 = enabled, 0 = disabled).
Q2M RxQual2 Mode (1 = Bipolar, 0 = differential).
IMEN+ Intermodule data+ enable (1 = enabled, 0 = disabled).
FPEN+ Front panel data+ enable (1 = enabled, 0 = disabled.)
IMEN- Intermodule data- enable (1 = enabled, 0 = disabled).
FPEN- Front panel data- enable (1 = enabled, 0 = disabled.)
CG Chassis ground (1 = relay connect signal and chassis ground, 0 = disconnect).
TEN0,TEN1 TTL output enable:

Bit 17	Bit 16	Signals Enabled
0	0	None
0	1	RxTrigValid, RxTrigNum0RxTrigNum3, RxSig1,RxSig2
1	0	RxG0Val, RxG1Val, RxClkOut
1	1	All

CS0,CS1 Clock select:

Bit 19	Bit 18	Clock
0	0	RxClkIn1
0	1	RxClkIn2
1	0	Intermodule Clock
1	1	None

LEDEN Front panel led enable (1 = enabled, 0 = disabled).

Notes:

1. LEDEN should only be enabled if RxSig1 = RxArm and RxSig2 = RxBusy.

2.2 RX01 Module ID (MID, R:178000$_h$)

The module ID register contains the RX01 ID code.

Table B-9 lists the bit description of the ID register.

Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU								T/R	T/P	ID					

Table B-9 RX01 Module Identification Register Bit Description

Field Bit Definition:

ID Identification code.
T/P Test/Production flag (1 = Test, 0 = Production).
T/R Transmit/Receive (1 = Receiver, 0 = Transmitter).

Notes:

1. A read of the MID register for the RX01 will return a ‘129’, 81_h.